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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-27,31-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-27,31-40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed May 28, 2004 has been entered. Claims 1, 3, 7, 8, 14, 18, 22, 24-26, 31, 34, 35, 38, 42 and 43 have been amended. Claims 1, 3-27, 31-40, 42 and 43 are pending.

Specification

2. In light of the Remarks filed May 28, 2004, the disclosure is objected to because of the following informalities:

The terms "selected to" according to the Remarks, means "slower".

However, specification, page 14, lines 14-25, discloses: "a first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about **2:1** selective to isolation film 36 as compared to insulator island 22".

Which means the removal rate of film (oxide) 36 is faster (2:1) as compared to insulator island (nitride) 22.

Also note that, the CMP is directed to planarizing the isolation film 36, while the nitride layer 22 is used as an etch stop. (page 15, lines 9-10). This matter is well known in the art that the removal rate of the etch-stop layer must be slower than that of the upper layer.

The specification seems to self-contradicting.

Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "14" and "44" have both been used to designate "pad oxide layer".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In Fig. 7B, "pad oxide", layer formed between polysilicon island 24 and substrate 12, is denoted as "14". While in Fig. 8B, the same layer, pad oxide, is now denoted as "44".

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming **said liner** upon side sidewall of each said isolation trench comprises **deposition** of a composition of matter" (claim 23) No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 14-23, 25-27, 31-40 are objected to because of the following informalities:

Claims 14, 18, 25, 26, 31 and 35, 38 recite: "wherein a material that is electrically insulative" and "wherein an electrically insulative material", respectively.

There is no nexus between this material and any layers in the body of the claims.

As corrected in claims 1 and 7, theses claims, 14, 18, 25, 26, 31, 35 and 38 should be corrected as well.

Therefore, the correct limitation should be: wherein the conformal layer comprises a material that is electrically insulative ...

Appropriate correction is required.

6. Claim 23 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 23 depends on claim 21. The limitations of claim 21 include: "said liner being confined within each said isolation trench and extending from an interface thereof".

However, claim 23 recites: "forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter".

As a matter of facts, a deposited layer would not being confined within the trench but all over the surface, inside and outside of the trench.

Thus, claim 23 is not just fails to further limit claim 21, but also contradicting claim 21.

7. Claim 34 is objected to because of the following informalities:

Claim 34, line 7, recites: "a layer composed of polysilicon upon said **gate** oxide in contact with a pair of said spacers".

However, as shown in Fig. 8B, the polysilicon layer 24 is formed on the pad oxide, not gate oxide.

As shown in Fig. 7B, the polysilicon 24 is formed upon the pad oxide 14.

With respect to Fig. 8B, this figure is an enlargement of Fig. 7B, upon which the nitride island 52 is removed. Note that Figs. A and B are directed to different embodiments.

The **gate** oxide 44 was **not** formed until all of the layers have been removed. (See page 19, lines 15-16).

Therefore, the correct term should be "a layer composed of polysilicon upon said oxide layer".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1 and 3-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which **was not described in the specification** in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a **written description** of the claim limitation "**so as to define an upper surface contour** of the conformal laver; and planarizing the conformal layer **beginning with the upper surface contour** of the conformal layer and extending at least to the first dielectric laver" (as recited in amended claims 1) in the application as filed.

Applicants **should point out a specific portion of the as-filed specification that directs to** "defining the contour of the upper surface of the dielectric layer, and the planarizing beginning with the upper surface contour".

At best, the specification discloses: "isolation film 36 **are planarized** to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process" (page 14, lines 14-17).

9. Claims 14-27, 31-40 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which **was not described in the specification** in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a **written description** of the claim limitation "planarizing is performed **in the absence** of masking the conformal layer over each said isolation trench" in the application as filed. The same had been rejected in the previous Office Action.

MPEP 2173.05(i) states: "The mere absence of a positive recitation is **not** basis for an exclusion. Any claim containing *a negative limitation* which *does not have basis in the original*

disclosure should be rejected under **35 U.U.C. 112, first paragraph** as failing to comply with the written description requirement". (See *In re Schechter,* 205 F.2d 185, 98 USPQ 144 (CCPA 1953); *Ex parte Parks*, 30 USPQ2d, 1234, 1236 (Bd. Pat. App. & Inter. 1993).

Applicants **should point out a specific portion of the original specification that directs to** "planarizing is performed **in the absence** of masking the conformal layer".

10. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "**rounding the top edge of the trench**" by thermally grown oxide from the substrate, does not reasonably provide enablement for *rounding the top edge of trench* by **deposition of a composition of matter** on the trench surface. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The specification clearly indicated that the rounding of the edge at the top of the isolation trench is a result of thermal oxidizing of the sidewall 50 to form the insulation liner 30. (See page 12, 1st paragraph). Further, as an alternative, the insulation liner can be formed by CVD (chemical vapor deposition).

Note that, rounding of the corner is a result of thermal oxidation, forming the thermal liner. When the insulation liner forms by CVD, the CVD is deposited on the etched trench which have not been rounded by the oxidation. Therefore, depositing the insulation liner by **CVD** does not result in rounding the corner and rounding the corner is not formed by CVD.

The specification ***fails to provide support*** for rounding the top edge of the trench by deposition of a composition of matter (CVD).

It is well known in the semiconductor technology that by consuming silicon at the corner during the thermal oxidation, the top edge of the trench becomes rounded.

Deposition, e.g. CVD, **does not consume any material** from the silicon substrate. Therefore, rounding does not occur.

How can the edge of trench be rounded when the liner is formed by deposit ?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 9, 10, 12, 13, 26 and 27 are further rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 9, 10, 12, 13, 26 and 27 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification filed September 8, 1999. In the specification, page 14, lines 14-25, applicant has stated "*Figure 7A illustrates a subsequence step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will be selective to isolation film 36, and relatively slightly selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly*

selective to spacer 28 over insulator island 22.", and this statement indicates that the invention is different from what is defined in the claim(s) because said passage means: **isolation film 36 is etch faster than the insulator island 22**, while claim 9 recites: "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said *first dielectric layer* (insulator island 22) *faster than said conformal layer* (isolation film 36) *and said spacers* (28) by a ratio in range from of about 1:1 to about 2:1.

Clearly, claim 9 is contradicting the disclosure, thus, fails to correspond to the scope of the invention.

Similar subject matter also recite in claims 10, 12, 13, 26 and 27.

As best understood by the examiner, the upper surface of each isolation trench is formed by an etch process using an etch recipe that etches the conformal layer 36 and spacers 29 faster than the insulator layer 22.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. Claims **1**, 3-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor et al. (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540) (all of record).

With respect to claim **1**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a second dielectric layer (352) over the oxide layer (340) and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second dielectric layer (352) over and in contact with the exposed oxide layer (340) at the plurality of areas; (Fig. 3G);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer (352), wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas; (Fig. 3H);

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench (360) is adjacent to and below the pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench (360) has a top edge; (Fig. 3I);

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364); (Fig. 3J); and

planarizing the conformal layer (364) beginning with the upper surface contour of the conformal layer (364) and extending at least to the first dielectric layer (344) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces;

wherein the conformal layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a liner upon the sidewall and rounding the top edge of the isolation trench (360).

However, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench-etch and inherently rounding the trench corner. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch.

With respect to claim 3, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate. (See Fig. 4).

With respect to claim 4, the liner of Poon comprises deposition of a composition of matter (50). (See Fig. 11).

With respect to claim 5, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of further includes forming a doped region below the termination of each isolation trench.

However, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region below the termination of each isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the inversion.

With respect to claim 6, the upper surface for each isolation trench (376) of Omid-Zohoor is formed by CMP. (See Fig. 3M, col. 4, ll. 47-62).

With respect to claim **7**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer (356) is situated upon the oxide layer

(340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below the pair of the spacers (356) and is situated at the corresponding area of the plurality of areas;

filling each the isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal layer and the depositing is carried out to the extent of filling each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) to a first thickness of the conformal layer (364) relative to the spacers (356) and the first dielectric layer (344);

planarizing the first thickness of the conformal layer (364) to a second thickness to form therefrom an upper surface for each of the isolation trench (360) that is co-planar to the other upper surfaces, wherein:

the conformal layer (364) comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches (360);

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer (364) and the spacer (356) and being situated above the oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the oxide layer (340). (See Figs. 3A-M).

With respect to rounding the top edge of each isolation trench or the formation of the liner, the similar reason as that of claim 1 is also applied here.

With respect to claim 8, the method of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claims 9 and 10, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed in an etch process using an etch recipe that etches the conformal layer (372) faster than the first dielectric layer (344).

With respect to claim 11, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed including:

chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; (Fig. 3M); and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer (340). (Fig. 3N).

With respect to claims 12 and 13, as best understood by the examiner, the etch that forms a second upper surface is well known in the art to etch the first dielectric layer (344) faster than the conformal layer (364) and the spacers (356).

With respect to claim **14**, as best understood by the examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer (340) and the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming a first silicon dioxide layer (252) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer (352), wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the silicon nitride layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate (120), wherein each isolation trench (360) is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second silicon dioxide layer (364), and the depositing is

carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and the silicon nitride layer (344); and

selectively removing the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the oxide layer (340), wherein the conformal second silicon dioxide layer is an electrically insulative extends continuously between and within the plurality of isolation trenches, and wherein the selectively removing is performed in the absence of masking the conformal second dioxide layer (364) over each isolation trench. (See Figs. 3A-M).

With respect to forming an electrically active region below the termination of each isolation trench (or doped region) and forming a liner upon the sidewall of each isolation trenches, respectively, the similar reasons as that of claims 5 and 1, respectively, are also applied here.

With respect to claim 15, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner of Poon is also composed of silicon nitride (50).

With respect to claim 17, the process of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120). (See Fig. 3P).

With respect to claims **18** and **24**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356),

wherein filling is performed by depositing the conformal third layer (364), and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer (364) to form therefrom the upper surface for each isolation trench that is co-planar to the other upper surface further comprises planarizing the conformal third layer (364) and each spacers (356) to form therefrom the co-planar upper surfaces, and planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

With respect to rounding the top edge of each isolation trenches, the similar reason as that of claim 1 is also applied here.

Further, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also,

Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to claim 19, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by CMP.

With respect to claim 20, a similar reasoning as that of claim 5, a doped region below the termination of each isolation trench, is also applied here.

With respect to claim 21, the process of Omid-Zohoor '072, in view of Poon, further comprises: prior to filling each isolation trench with the conformal third layer (364), forming a liner (28) upon the sidewall of the isolation trench to remove damage caused by the trench etch, the liner (28) being confined preferentially within each isolation trench (Fig. 4) and extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate, and wherein the conformal third layer (364) is composed of electrically insulative material.

With respect to claim 22, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 23, as best understood by the examiner, forming the liner upon the sidewall of the isolation trench of Poon also comprises deposition of a composition of matter (50).

With respect to claim **25**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation

trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein the conformal third layer comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Fig. 3A-M).

With respect to rounding the top edge of each isolation trenches, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim **26**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation

trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) by an etch using an etch recipe that etches the first dielectric layer (344) slower than the conformal third layer (364) and the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

wherein the conformal third layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trench. (See Figs. 3A-M).

With respect to rounding the top edge of each isolation trenches, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim 27, as best understood by the examiner, in the planarizing of the conformal third layer (364), the conformal third layer (364) is removed faster than the first dielectric layer (344). (See Fig. 3M).

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer (344) to exposed the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the pad oxide layer and over the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming the first silicon dioxide layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer (356) is situated upon the pad oxide layer, is in contact with the silicon nitride layer (344) and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344); and

planarizing the conformal second layer (364) and each of the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface and is situated above the pad oxide layer (340), wherein the planarizing is performed in the absence of masking the conformal second layer (364) over each of the isolation trenches;

wherein the conformal second layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

With respect to removing the silicon nitride layer and the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to forming of the doped region, the liner and rounding the top edge of the isolation trench, the similar reasons as that of claims 1 and 5 are also applied here.

With respect to claim 32, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 33, as best understood by the examiner, the liner of Poon is also composed of silicon nitride (50) and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, the method of Omid-Zohoor further comprises: (also see claim 25):

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (see Fig. 3N);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120); (see Fig. 3P);

forming between the isolation trenches (360), and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces. (See Fig. 3N).

13. Claims **35**-40, **42** and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55 (of record).

With respect to claim **35**, as best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll.14-16);

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first layer (344);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by planarizing in the absence of masking the second layer over each of the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to remove damage caused by the trench etch. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

With respect to selectively removing the first layer and the polysilicon layer to exposed the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim 36, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type (n-type) to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 2-37).

With respect to claim 37, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **38**, as best understood by the examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon; (Fig. 3B);

forming a first layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a plurality of isolation trenches (360) through the oxide layer (340) at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344); (Fig. 3H);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356); (Fig. 3I);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356), wherein the filling is performed by depositing the second layer (364), and the depositing is carried out to the extend of filling

each isolation trench and extending over the spacer (356) and over the first layer (344); (Fig. 3J);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is formed by planarizing in the absence of masking the second layer (364) over each of the isolation trench; (Fig. 3M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

With respect to the top edge being rounded, a similar reason as that of claim 35 is also applied here.

With respect to claim 39, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type (n-type) to form a doped trench bottom that is below and in contact with a respective one of isolation trenches. (See Fig. 2-37).

With respect to claim 40, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **42**, As best understood by examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll. 14-16);

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trenches and extending over the spaces (356) and the first layer (344); and

forming with a single etch recipe a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

With respect to rounding the top edge of the isolation trench, a similar reason as that of claim 35 is also applied here.

With respect to claim **43**, as best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344); and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation structures, and being situated above the oxide layer, wherein planarizing is performed in the absence of making the conformal layer over each of the isolation trenches, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

With respect to the rounding of the top edges of the isolation trench, a similar reason as that of claim 35 is also applied here.

Response to Arguments

14. Applicant's arguments filed May 28, 2004 have been fully considered but they are not persuasive.

Objection to the Drawings

Fig. 5A and 5B, only show a liner (30) which are formed by thermally grown, not deposit. As discussed above, a liner if formed by deposit, should extend over the substrate as shown in Fig. 3I of patent No. 6,184,108. The objection is maintained.

Claim Rejection Under 35 U.S.C. 112, first paragraph:

With respect to new matter "planarizing is performed in the absence of masking the conformal layer over the isolation trench", through a lengthy argument, applicant still fails to

point out the specific disclosure regarding the planarizing is performed in the **absence** of masking the conformal layer.

The Applicants appear to claim what they do not invent, rather than claim what they do invent.

As discussed above, a positive recitation in the specification is required for a negative limitation claim. (See MPEP 2173.05(i)).

With respect to the rejection of claim 23 for does not reasonably provide enablement for the liner being formed by deposit so that the top edge of the isolation trench become rounded, the Applicants state: "Applicants respectfully traverse", but do not advance any reason.

The rejection is thus, maintained.

Rejection Under 35 U.S.C. 112, second paragraph:

With respect to claims 9, 10, 12, 13, 26 and 27, Applicants cited page 15, lines 11-15, and defined: the term "selective to" means the layer is etched slower than other materials.

However, page 14, lines 14-25 teaches the contrary: "a first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about **2:1** selective to isolation film 36 as compared to insulator island 22".

Which means the removal rate of film (oxide) 36 is **faster** (2:1) as compared to insulator island (nitride) 22.

On the other hand, page 15, lines 11-15, fails to provide an etch ratio for "slower" selective to.

The rejection is therefore, maintained.

Rejection under 35 U.S.C. 103(a)

Regarding claim 1, the Applicants argue: the method disclosed in the '072 patent does not teach or suggest planarizing the conformal layer "beginning with the upper surface contour of the conformal layer" as recited in claim 1.

First of all, the specification fails to support the new matter "beginning with the upper surface contour of the conformal layer".

Secondly, it is obvious that the planarization of '072 can not start in the **middle** of the layer, hence, it must be from the top.

Thirdly, the planarization of '072 clearly encompasses the limitation of "planarizing the conformal layer beginning with the upper surface contour of the conformal layer", because it does not matter how the conformal layer 364 is etched, the planarization has to start from the top surface.

Regarding claim 7, the same response also applies, since the Applicants only repeat the argument of claim 1.

Regarding claims 18 and 24-26, the Applicants appear to contend that: '072 patent does not teach a planarization that is performed in the absence of masking of a conformal layer.

As discussed many time before and now repeated, the as-filed specification fails to support the new matter of "planarization that is performed in the absence of masking".

Additionally, in '072 patent, there is no mask present during the CMP (planarization) of the conformal layer 364. (See Figs. 3L-M).

Regarding claim 31, the Applicants appear to repeat the same argument as that of claim 18 and further add: the '072 patent discloses a more complicated method that involves masking of conformal layer.

Note that, the more complicated method does not mean that '072 patent does not planarize the upper surface of the conformal oxide layer.

Regarding claim 34, since the pad layer of '072 includes: an oxide and a polysilicon layers, thus, the limitation of claim 34 is met. Furthermore, as discussed in the objection above, the claimed matter contradicting and fail to have support in the specification.

Regarding claims 35-40, 42 and 43, the Applicants argue: '072 patent has no teaching or suggestion of this feature, "forming a polysilicon upon an oxide layer".

As had discussed many time before, as an alternative, '072 patent teaches: "a pad oxide containing a thin thermally-grown silicon oxide layer and a buffer polysilicon layer may be used for the pad oxide 340". (See col. 4, lines 11-16).

The Applicants further repeat the argument of "planarization in the absence of masking of the conformal layer".

The Office is respectfully direct the Applicants to the discussion above regarding this subject matter.

Regarding claim 43, the Applicants appear to contend that '072 patent does not teach "planarizing the conformal layer ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces".

The Office is respectfully direct the Applicants to Fig. 3M, wherein after the planarization of the conformal layer (364), the upper surface for each isolation trench that is co-planar to the other upper surfaces are formed.

The Applicants further repeat the argument of "planarization in the absence of masking of the conformal layer".

The Office is respectfully direct the Applicants to the discussion above regarding this subject matter.

Regarding claim 42, the Applicants argue: in contrast, '072 patent uses a multi-step method with different etch recipes to form a planar upper surface.

Contrary to the Applicants assertion, the CMP to form the planar upper surface of '072 is only a single etch recipes. (See Figs. 3L-M).

'072 patent in view of Poon or Wolf clearly render the claims obvious because thermal oxidizing the exposed trench to remove damage caused by the trench etch are well known in the art.

The claims are obvious over the combination of the references.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh D. Mai
September 7, 2004